

OVERVIEW

The CL12911IP4000 is based on MIPI A-PHY interface specification announced in year 2020, targeting ultra-high-speed networking applications in ADAS and autonomous drive subsystems. It supports applications that require long reach (up to 15 meters), error-free links, and high EMI immunity requirement.

PHY IP supports the SOURCE function of MIPI A-PHY Gear-2 / Profile 1 stated in standard specification. It supports data rate up to 4Gbps with integrated mixed signal circuit, high performance TX driver, embedded TX clock generation, on chip optional termination resistor calibration.

This CL12911IP4000 A-PHY Source IP enables designers with the low area and low power with support for the leading process technologies in TSMC Foundry 40nmLP process.

FEATURES

- Compliant with MIPI A-PHY specification version 1.1
- Support Gear-2 Profile 1 up to 4Gbps
- Support data bus width: 20-bit parallel interface
- Support 1 lane
- Support Uplink Receiver @ 100Mbps
- Selectable input clock frequency: 25MHz
- Maximum output clock frequency at 200MHz
- Supports Single-ended coaxial or shielded twisted-pair (STP) cable up to 15m
- support A-PHY PMD layer by HARD macro
- High performance Data and clock recovery.
- Analog monitor port for test and debug
- Embedded termination Resistor and optional calibration function
- Supporting Link IP CD12911IP200 (PHY layer PCS, RTS and Data Link) soft macro Native Protocol Adaption layer supports (Option)

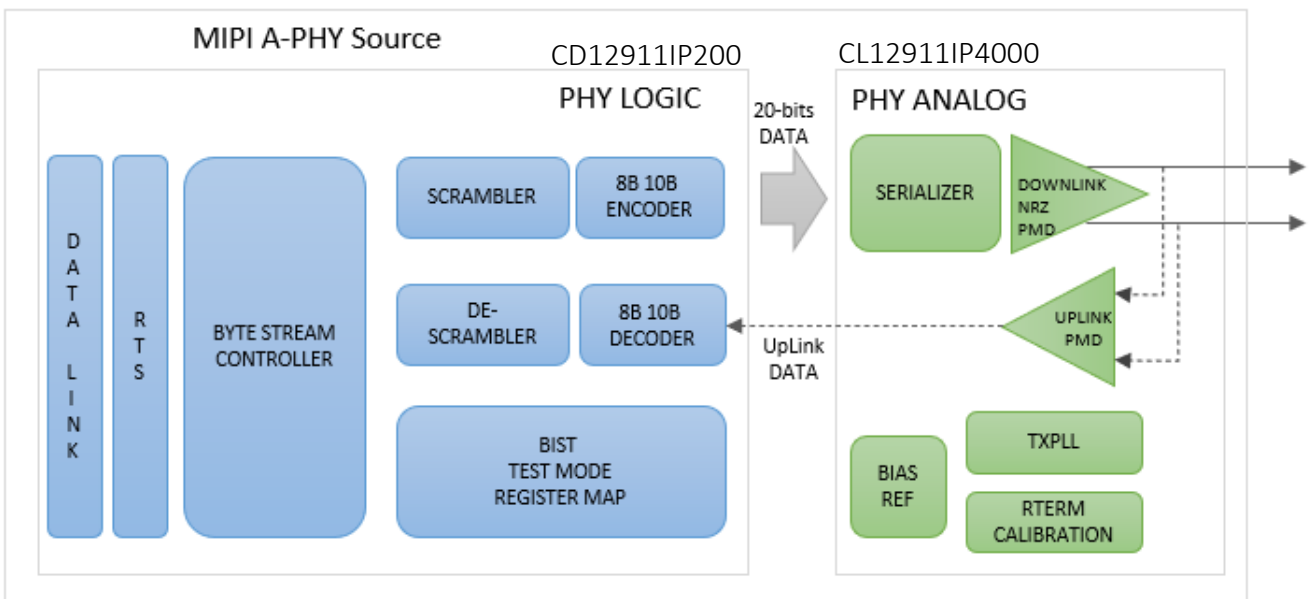


Figure 1 Generic block diagram of CL12911IP4000 and CD12911IP200

CL12912IP4000 – SENSOR/DISPLAY MIPI A-PHY SINK IP

Parameters		Specification
Technology Node		TSMC 40nm LP
Compliance / Standard		MIPI A-PHY V1.1
Input Reference Clock		25MHz
Data Rate		≤ 4 Gbps
Number of Pad Required		
Signals		2
Monitor/calibration		2
Power/Ground		5
Operating Condition	VDD11	0.99V ~ 1.21V
	VDD18	1.62V ~ 1.98V
	Temperature	-40C ~ 125C
IP Size (PHY Analog)		~ 800um x 700um

DELIVERABLES

- GDSII & layer map
- Place-Route views (.LEF)
- Liberty library (.lib)
- Verilog behavior model
- Netlist & SDF timing
- Layout guidelines, application notes
- LVS/DRC verification reports
- Test patterns and Test Documentation

CURIOUS is a leading fabless design house specializing in high-speed interface IP and mixed signal module for Image Sensors, Display and Data application.

For more information about CURIOUS IP, visit

<https://www.curiousstek.com>

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We can provide process porting and lane customization.

If you have any questions or requirements,

such as a detailed information of Curious IP products,

please contact us at the email address : curious.info@curious-jp.com