Introduction

The CL12842M8RM3AM5AIP5000 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to ISP (Imaging Signal Processer) and DSP. The CL12842M8RM3AM5AIP5000 is designed to support data rate in excess of maximum 5Gbps utilizing SLVS-EC ver.2.0 / MIPI D-PHY ver.1.2 / HiSPi / sub-LVDS / CMOS 1.8V interface specification. The CL12842M8RM3AM5AIP5000 can change Interface type using same PAD by changing mode.

Feature

- SLVS-EC ver.2.0 / MIPI D-PHY ver.1.2 compliant
- Supporting for five kind Differential Input Signals
  - 1) SLVS-EC (Maximum 5.0Gbps)
  - 2) MIPI D-PHY (Maximum 2.5Gbps)
  - 3-1) sub-LVDS (Maximum 1.0Gbps)
  - 3-2) sub-LVDS(P) (Maximum 1.386Gbps)
  - 4) HiSPi (Maximum 700Mbps)
  - 5) CMOS 1.8V (Maximum 166MHz)
- Xtal Input Clock Frequency Selectable
  - 25MHz /50MHz / 75MHz @ 5Gbps (2.5Gbps, 1.25Gbps)
  - 37.125MHz /54MHz @ 4.752Gbps (2.376Gbps, 1.188Gbps)
  - 24MHz /48MHz / 72MHz @ 4.608Gbps (2.304Gbps, 1.152Gbps)
- Maximum Output Clock Frequency
  - ~250MHz @ SLVS-EC, Select parallel data bus width to 20bit
    ~500MHz @ SLVS-EC, Select parallel data bus width to 10bit
  - ~312.5MHz @ MIPI D-PHY
- Power Supply:
  - Vcc=1.8V (IO and Analog) Vdd=0.80 V (Inside Core) @12nFFC
  - Vcc=1.8V (IO and Analog) Vdd=0.75 V (Inside Core) @7nFFC
- Maximum Lane Number: 8-Lane
- 10/20-bit/Lane Parallel Outputs (SLVS-EC)
  8-bit/Lane Parallel Outputs (sub-LVDS / MIPI D-PHY / HiSPi)
- Including Power Down Mode
- Including Differential Low Detect Circuit for SLVS-EC
- TSMC 12nm FFC Process Metal code 1P11M_2Xa1Xd_h_3Xe_VHV_2Y2R
  TSMC 7nm FF Process Metal code 1P13M_1X_1Xa_1Ya_5Y_2Yy_2R
  (Using of Standard Vth and Low Vth and ultra-Low Vth Transistor)
- IO Direction: South-North

Support Link controller

- CD12842 Link controller (Ready)

We can provide process porting and lane customization.
If you have any questions or requirements,
such as a detailed information of Curious IP products,
please contact us at the email address : curious.info@curious-jp.com