Overview

1.1 Description

The CL12811M8TIP10000 TXPHY supports 8 TX DATA lanes for up to 10Gbps application. A wide range phase-locked clock is embedded in the IP to support multi data rate configuration. The CL12811M8TIP10000 transmitter supports the function that the polarity of differential signals for each data lane can be controlled. The CL12811M8TIP10000 transmitter is an ideal hard macro to solve EMI and interface size issues associated with high speed CMOS interface.

1.2 Feature

- SLVS-EC ver.3.0 compliant
- Data Rate: Up to 10Gbps / lane
- Number of data lane: 8
- Support input clock: 24MHz, 54MHz, 37.125MHz, 72MHz, 74.25MHz
- Polarity of TX differential output for each data lane is programmable.
- Integrated wide range Phase Lock Loop
- 4-bits programable level of output differential voltage
- Support BIST function for at-speed loopback test
- Selectable data bus mode, 10-bit, 20-bit and 40-bit

1.3 Technology

Process option:	TSMC12FFC
Metal Stack:	1P11M_2Xa1Xd_h_3Xe_VHV_2Y2R
IO Direction:	North-South

1.4 Support Link controller

- CD12811 Link controller (In planning)

Block Diagram

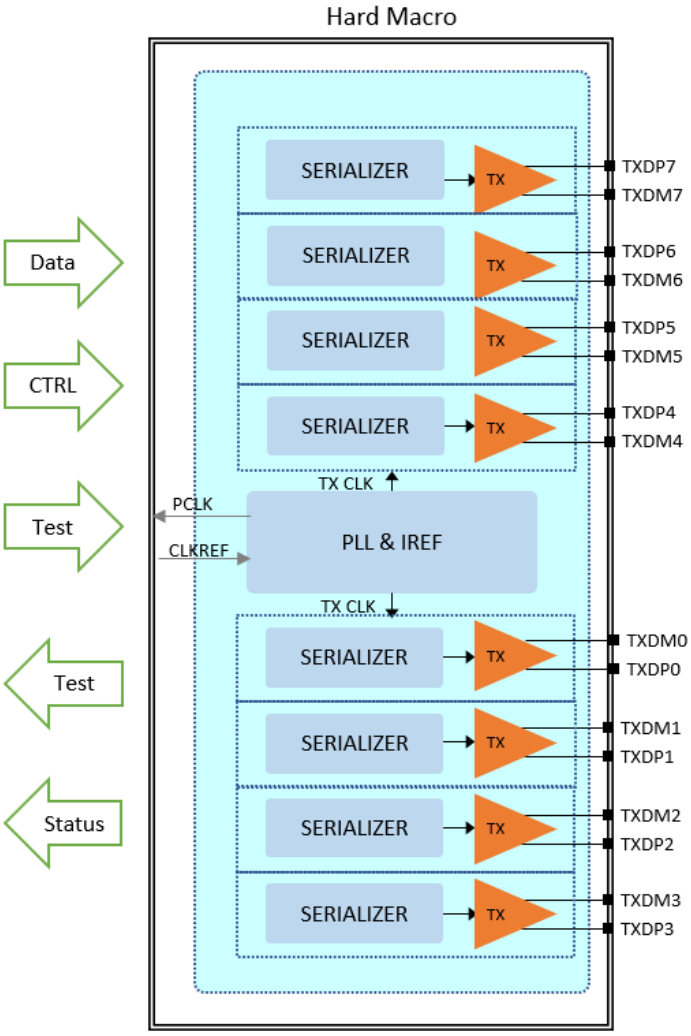

Figure 2.1 Overall block diagram of TX

We can provide process porting and lane customization.
If you have any questions or requirements,
such as a detailed information of Curious IP products,
please contact us at the email address : **curious.info@curious-jp.com**