1 Overview

1.1 Description

The LVDS/Sub-LVDS/DPHY Combo TX converts parallel RGB data and 7/8/10 bits of CMOS parallel data into serial data streams. A phase-locked clock is transmitted in parallel with the data streams over a dedicated high-speed link. The polarity of differential signals for each data lane can be controlled. The CL12661M10T2DM2FIP transmitter is an ideal means to solve EMI and cable size issues associated with high-speed CMOS interface.

1.2 Feature

- Data Rate: Up to 1.0 Gbps for LVDS, sub-LVDS / 2.5 Gbps for DPHY
- Clock polarity programmable
- Data polarity for each data lane is programmable
- Integrated Integer-N PLL
- 4 programable level of output differential voltage
- BIST function for loopback test
- Operational modes supported:
  - to support LVDS dual link (5 data lanes + 1 clock lane) x 2 channel
  - to support sub-LVDS dual link (5 data lanes + 1 clock lane) x 2 channel
  - to support DPHY @ 2.5Gbps (4 data lanes + 1 clock lane) x 2 channel

1.3 Technology

Process option: TSMC 6FFC
Metal Stack: 1P13M_1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy_2Z_UTALRDL

1.4 Support Link controller

- CD12611 Link controller (Ready)

2 Block Diagram

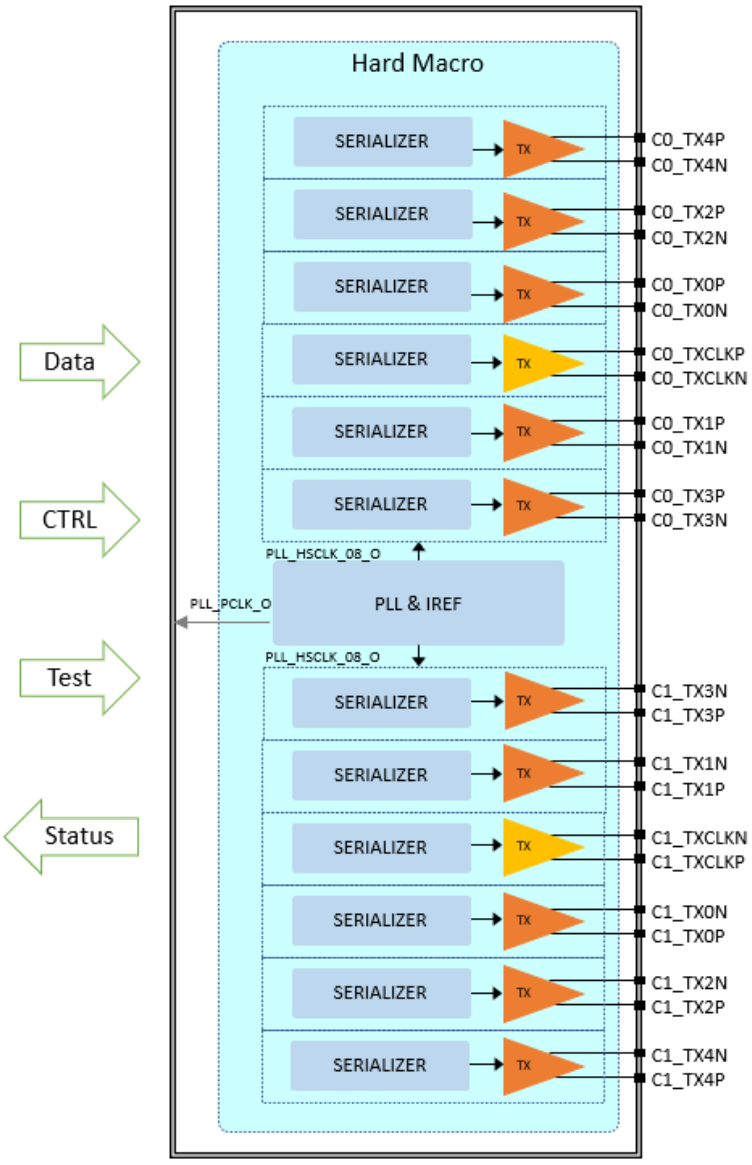

Figure 2.1 Overall block diagram of CL12661M10T2DM2FIP

We can provide process porting and lane customization.
If you have any questions or requirements,
such as a detailed information of Curious IP products,
please contact us at the email address : **curious.info@curious-jp.com**