Introduction

The CL12631I4T1AS1BIP2500 is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System.

The CL12631I4T1AS1BIP2500 converts the input parallel data to the serial data and output it.

The CL12631I4T1AS1BIP2500 is designed to support maximum 2.5Gbps data rate utilizing mipi-DPHY specification v1-2.

Feature

- MIPI-DPHY v1-2 / MIPI CSI2 compliant
- Supporting Differential Output Signals: MIPI-DPHY (Maximum 2.5Gbps)
- (MIPI-DPHY 8bit SER) PCK $N = \sim 313$ MHz Input Clock Frequency:
- Output Clock Frequency: ~1250MHz Output Data Rate: ~2.5Gbps
- Power Supply: 2.8V, 1.2V(PLL/BGR) 1.2V(PHY)
- Max TX Lane Number: Clock 1-port / Data 4-ports (lanes)
- Data Input Path: 8bit Parallel
- Include Power Down Mode
- Include Output clock's On/Off Mode
- Include Dp, Dm polarity Control
- TPSCo 65nm BSB Process
 - Triple well structure Layer: $7M/1L (1M \sim 6 M, 9M, L)$ 1.2V / 3.3V Transistor
- Various process porting support available (Please contact us.)
- Supporting Link-layer (Soft Macro):
 - CD12631

If you have any questions or requirements, such as a detailed information of Curious IP products, please feel fee to contact us at the email address: curious.info@curious-jp.com