CL12491M8TIP160: LVDS 160MHz 8-Lane PHY TX IP

1 Overview

1.1 Description

The CL12491M8TIP160 transmitter converts parallel RGB data and 4bits of HYNC,VSYNC,DE and Control) of CMOS parallel data into serial LVDS data streams. A phase-locked clock is transmitted in parallel with the data streams over a dedicated LVDS link. The polarity of differential signals for each data lane can be controlled. The transmit clock frequency of 160MHz, 24bits RGB data, and 4bits LCD timing & control data (HSYNC, VSYNC, DE,Control1) are transmitted at the rate of 1.12Gbps per LVDS data lane. The CL12491M8TIP160 transmitter is an ideal means to solve EMI and cable size issues associated with high-speed CMOS interface.
The CL12491M8TIP160 has integrated PLL with spread spectrum clock option. The targeted SSC modulating frequency is designed to be in the range of 10KHz ~ 30KHz, with modulation depth up to 3.1%, centered spread.

1.2 Feature

- Data Rate: Up to 1.12Gbps
- Clock polarity programmable
- Data polarity for each data lane is programmable
- Integrated PLL with spread Spectrum option
- 4 programable level of output differential voltage
- RX detection circuit to detect connectivity to device
- Clock-in-fail detection to detect malfunction of clock source
- BIST function for loopback test
- Operational modes supported:
  - to support 1080p@60fps with single link (4 data lanes + 1 clock lane)
  - to support 2560x1440 @60fps with dual link (8 data lanes + 1 or 2 clock lane)

1.3 Technology

Process option:	TSMC16FFC
Metal Stack:	1P10M_2Xa1Xd_h_4Xe_vhvh_2R_UT-APRDL

2 Block Diagram

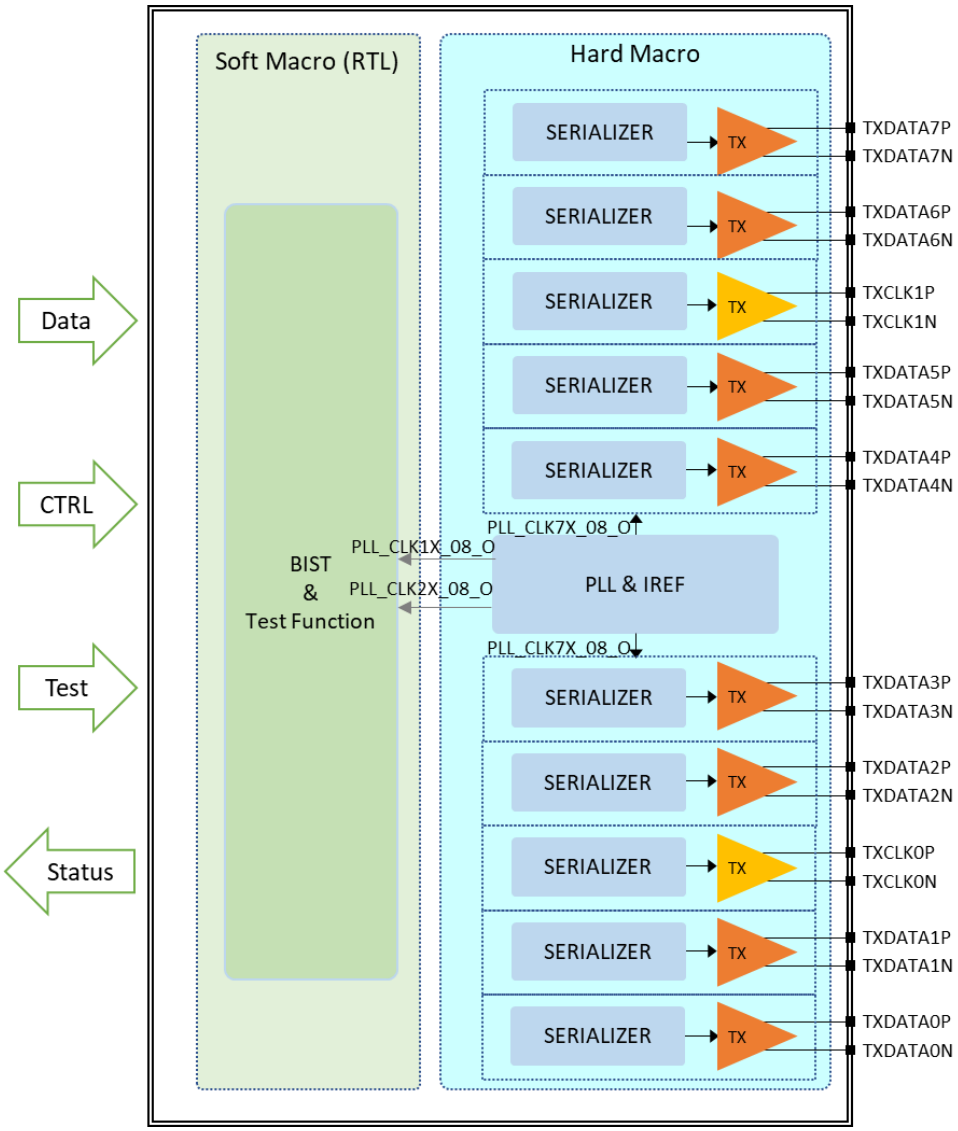

Figure 1 Overall block diagram of TX

We can provide process porting and lane customization.
If you have any questions or requirements,
such as a detailed information of Curious IP products,
please contact us at the email address : **curious.info@curious-jp.com**