

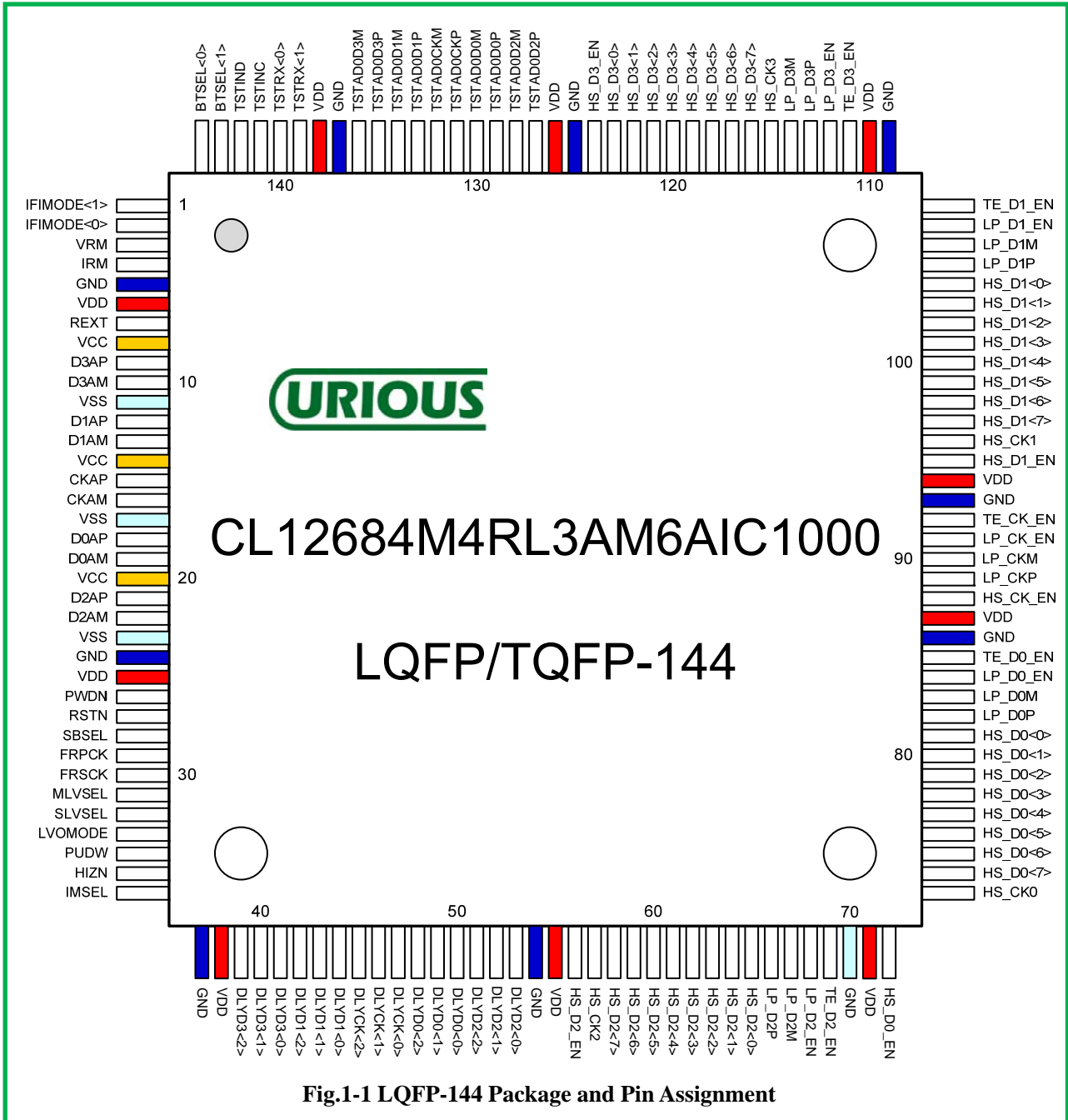
Introduction

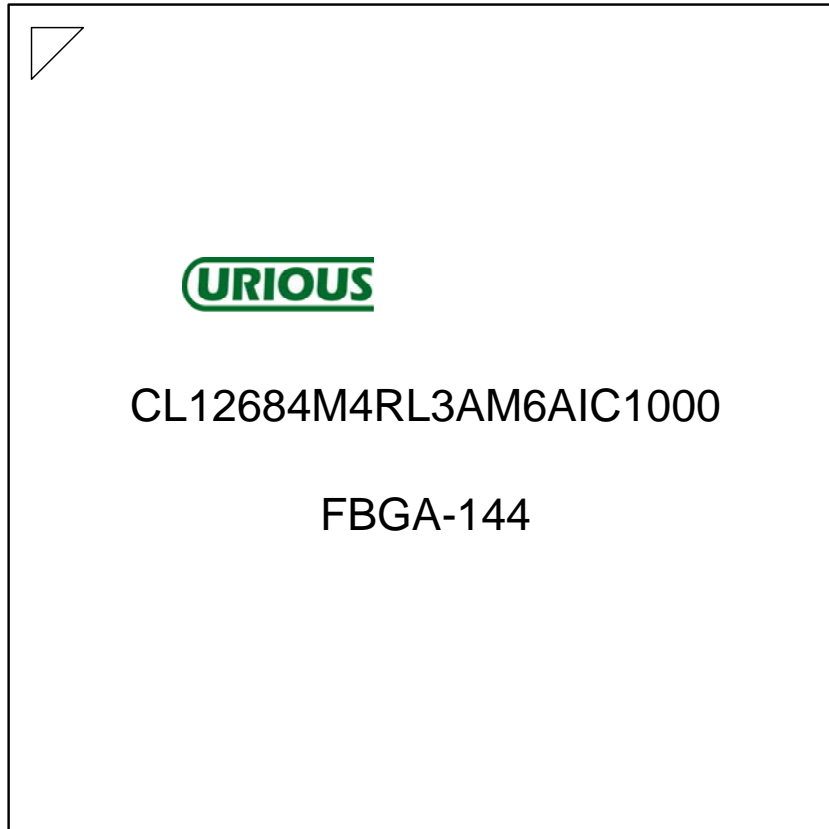
The CL12684MR3AM6AIC is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CL12684M4R3AM6AIC is designed to support data rate in excess of maximum 1Gbps utilizing sub-LVDS / mini-LVDS / LVDS / HiSPi(SLVS-400, HiVCM) / MIPI-DPHY / CMOS interface specification. The CL12684M4R3AM6AIC can change Interface type to same PAD for changing mode.

Feature

- MIPI DPHY v1-1 / MIPI CSI / TIA/EIA-644 LVDS / SLVS-400 compliant
- Differential signal of almost CIS serial and parallel inputs support
 - 1) sub-LVDS Serial / Parallel
 - 2) mini-LVDS (Reduce Mode LVDS) * SLVS-200
 - 3) LVDS
 - 4) HiSPi (SLVS-400, HiVCM)
 - 5) MIPI DPHY
 - 6) CMOS 1.8V
- LVDS 2bit serial outputs support for LVOMODE pin
- Differential inputs to LVDS outputs support for LVOMODE and TSTADOxx pin
- Maximum Input Clock Frequency: ~500MHz Maximum Input Data Rate: ~1Gbps
- Maximum Output Clock Frequency: ~500MHz Maximum Output Data Rate: ~500Mbps
- Power Voltage: Analog 1.8V / Digital 1.8V
- Maximum Serial Input Ports(Lanes): Clock 1-port / Data 4-ports (lanes)
- Output Serial Clock Edge Programmable for FRPCK pin
- Output Format 2/4/8bit Selectable for BTSEL[1:0]
- MSB/LSB Selectable for SBSEL pin
- Using for receiver of almost CMOS Image Sensor (Panasonic/Sony/Aptina/OVT/AltaSels/ST-micro e.t.c.)
- Power Consumption: (Process: FF, Temperature: 125, Power Voltage: max) $I_{TOTAL}=V_{CC}+V_{DD}$
 - Active maximum 100mA
 - Sleep maximum 10uA (for PWDN pin)
- ESD (HBM / MM / CDM / Latch Up): 2kV / 200V / 500V / 100mA

Package and Pin Assignment





	1	2	3	4	5	6	7	8	9	10	11	12
A	BTSEL[0]	BTSEL[1]	TSTIND	TSTRX[0]	TSTADOD3M	TSTADOD3P	VDD (D)	HS_CK3	LP_D3M	TE_D1_EN	HD_D3[3]	HD_D3[4]
B	IFIMODE[1]	IFIMODE[0]	TSTINC	TSTRX[1]	TSTADOD1M	TSTADOD1P	GND (D)	HD_D3[7]	LP_D3P	LP_D1_EN	HD_D3[2]	HD_D3[5]
C	VRM	IRM	REXT	VDD (D)	TSTADOCKM	TSTADOCKP	HS_D3_EN	HD_D3[6]	LP_D3_EN	LP_D1M	HD_D3[1]	HD_D3[6]
D	GND (D)	VDD (D)	VCC	GND (D)	TSTADOD0M	TSTADOD0P	HD_D3[0]	HD_D3[5]	TE_D3_EN	LP_D1P	HD_D3[0]	HD_D3[7]
E	D3P	D3M	VSS	LVOMODE	TSTADOD2M	TSTADOD2P	HD_D3[1]	HD_D3[4]	VDD (D)	GND (D)	HS_D1_EN	HS_CK1
F	D1P	D1M	VCC	PUDW	DLYCK[0]	DLYD0[2]	HD_D3[2]	HD_D3[3]	LP_CK_EN	TE_CK_EN	VDD (D)	GND (D)
G	CKP	CKM	VSS	HIZN	DLYCK[1]	DLYD0[1]	GND (D)	VDD (D)	LP_CKP	LP_CKM	VDD (D)	GND (D)
H	D0P	D0M	VCC	IMSEL	DLYCK[2]	DLYD0[0]	HS_D2[6]	HS_D2[5]	HS_CK_EN	HS_D0[6]	HS_D0[5]	TE_D0_EN
J	D2P	D2M	VSS	GND (D)	DLYD1[0]	DLYD2[2]	HS_D2[7]	HS_D2[4]	LP_D2_EN	HS_D0[7]	HS_D0[4]	LP_D0_EN
K	GND (D)	VDD (D)	FPSCK	VDD (D)	DLYD1[1]	DLYD2[1]	HS_CK2	HS_D2[3]	LP_D2M	HS_CK0	HS_D0[3]	LP_D0M
L	PWDN	SBSEL	MLVSEL	DLYD3[2]	DLYD1[2]	DLYD2[0]	HS_D2_EN	HS_D2[2]	LP_D2P	HS_D0_EN	HS_D0[2]	LP_D0P
M	RSTN	FRPCK	SLVSEL	DLYD3[1]	DLYD3[0]	GND (D)	VDD (D)	HS_D2[1]	HS_D2[0]	TE_D2_EN	HS_D0[1]	HS_D0[0]

Fig.1-2 FBGA-144 Package and Pin Assignment