

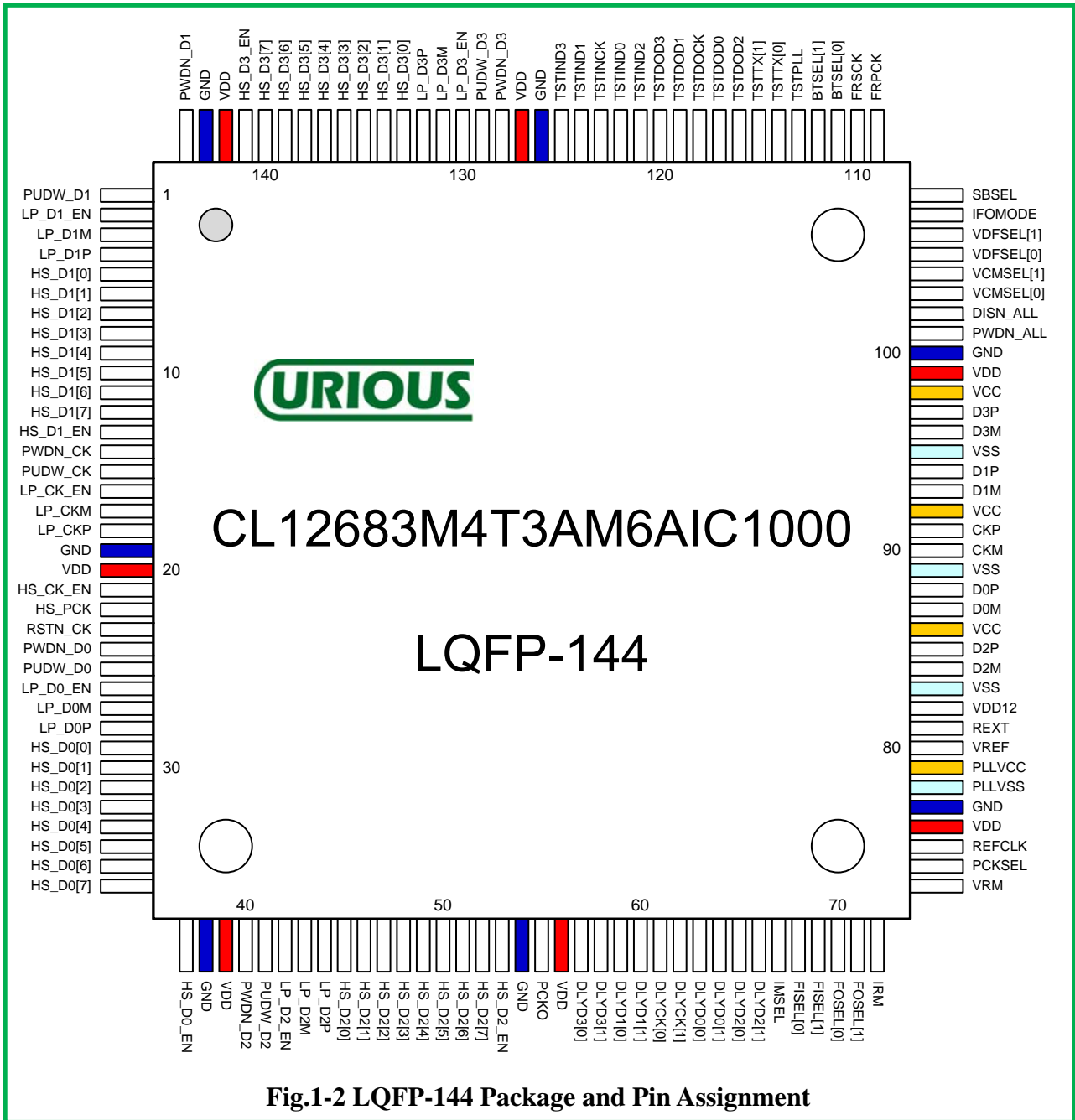
Introduction

The CL12683M4T3AM6AIC is an ideal means to link Camera Modules or CMOS Image Sensor (CIS) to Host System. The CL12683M4T3AM6AIC is designed to support data rate in excess of maximum 1Gbps utilizing sub-LVDS / mini-LVDS / LVDS / HiSPi(SLVS-400) / MIPI-DPHY / CMOS interface specification. The CL12683M4T3AM6AIC can change Interface type to same PAD for changing mode.

Feature

- MIPI DPHY v1-1 / MIPI CSI / TIA/EIA-644 LVDS / SLVS-400 compliant
- Differential signal of almost CIS serial outputs support
 - 1) sub-LVDS Serial / Parallel
 - 2) mini-LVDS (Reduce Mode LVDS)
 - 3) LVDS
 - 4) HiSPi (SLVS-400)
 - 5) MIPI DPHY (Maximum 4-Lane)
 - 6) CMOS 1.8V (Maximum 10MHz)
- Input Clock Frequency: ~125MHz Input Data Rate: ~250Mbps
- Output Clock Frequency: ~500MHz Output Data Rate: ~1Gbps
- Power Voltage: Single 1.8V
- Maximum Serial Input Ports(Lanes): Clock 1-port / Data 4-ports (lanes)
- Input Serial Clock Edge Programmable for FRPCK pin
- Input Format 2/4/8bit Selectable for BTSEL[1:0]
- MSB/LSB Selectable for SBSEL pin
- Power Consumption: (Process: FF, Temperature: 125, Power Voltage: max) $I_{TOTAL}=V_{CC}+V_{DD}$
 - Active maximum 100mA
 - Sleep maximum 10uA (for PWDN_ALL pin)
- ESD (HBM / MM / CDM / Latch Up): 2kV / 200V / 500V / 100mA

Package and Pin Assignment





1	2	3	4	5	6	7	8	9	10	11	12
PWDN_CK	HS_D1[3]	HS_D1[2]	PUDW_D1	HS_D3[1]	HS_D3[0]	TSTIND0	TSTIND2	FRSCK	FRPCK	VDFSEL[1]	VDFSEL[0]
PUDW_CK	HS_D1[4]	HS_D1[1]	PWDN_D1	HS_D3[2]	LP_D3P	TSTINCK	TSTDOD3	BTSEL[0]	SBSEL	VCMSEL[1]	VCMSEL[0]
LP_CK_EN	HS_D1[5]	HS_D1[0]	GND (D)	HS_D3[3]	LP_D3M	TSTIND1	TSTDOD1	BTSEL[1]	IFOMODE	NDIS_ALL	PWDN_ALL
LP_CKM	HS_D1[6]	LP_D1P	VDD (D)	HS_D3[4]	LP_D3_EN	TSTIND3	TSTDODCK	TSTPLL	VCC	VDD (D)	GND (D)
LP_CKP	HS_D1[7]	LP_D1M	HS_D3_EN	HS_D3[5]	PUDW_D3	GND (D)	TSTDOD0	TSTRX[0]	VSS	D3M	D3P
GND (D)	HS_D1_EN	LP_D1_EN	HS_D3[7]	HS_D3[6]	PWDN_D3	VDD (D)	TSTDOD2	TSTRX[1]	VCC	D1M	D1P
VDD (D)	LP_D0_EN	HS_D0_EN	LP_D2M	LP_D2P	VDD (D)	PCKO	IMSEL	FISEL[0]	VSS	CKM	CKP
HS_CK_EN	LP_D0M	HS_D0[7]	LP_D2_EN	HS_D2[0]	GND (D)	DLYD3[0]	DLYD2[1]	FISEL[1]	VCC	D0M	D0P
HS_PCK	LP_D0P	HS_D0[6]	PUDW_D2	HS_D2[1]	HS_D2_EN	DLYD3[1]	DLYD2[0]	FOSEL[0]	VSS	D2M	D2P
RSTN_CK	HS_D0[0]	HS_D0[5]	PWDN_D2	HS_D2[2]	HS_D2[7]	DLYD1[0]	DLYD0[1]	FOSEL[1]	VDD12	PLLVD (D)	PLLVS (D)
PWDN_D0	HS_D0[1]	HS_D0[4]	VDD (D)	HS_D2[3]	HS_D2[6]	DLYD1[1]	DLYD0[0]	IRM	REXT	VREF	GND (D)
PUDW_D0	HS_D0[2]	HS_D0[3]	GND (D)	HS_D2[4]	HS_D2[5]	DLYCK[0]	DLYCK[1]	VRM	PCKSEL	VDD (D)	REFCLK

Fig.1-3 FBGA-144 Package and Pin Assignment