

### Introduction

The CL12662IP Multi-Receiver convert MIPI –DPHY and SMIA CCP class 0, 1, 2 and DDR Clock/Data streams back into parallel 8-bits of LVCMOS. The output LVCMOS clock is transmitted in parallel with data. This chipset is an ideal means to link mobile camera modules Baseband processors. A configurable input pin (CLS) is provided to select different Class (0 or 1, 2) mode inside the SMIA standard specifications. And MIPI-DPHY and SMIA and DDR format mode support for mode pin (MDS). The CL12662IP Transmitter is an ideal means to solve EMI and cable size problems associated with wide, high speed CMOS interface.

### Feature

- Input Clock: 80MHz~500MHz,      Output Data Rate: 160Mbps~1Gbps
- Output Clock: 20MHz~125MHz shift clock support
- Differential Input, LVCMOS Output
- MIPI-DPHY Ver.1.00.00 / SMIA CCP Class0, 1, 2 compliant
- SMIA CCP Class0, CCP Class1, 2 supports (CLS pin)
- MIPI-DPHY / SMIA / DDR Format support (MDS pin)
- High Speed Rate
 

Serial Input:	MIPI-DPHY	~1Gbps (Data0~n+/-, Clk+/-)
	SMIA CCP Class0	~208Mbps (Data0~n+/-, Clk+/-)
	SMIA CCP Class1, 2	208~650Mbps (Data0~n+/-, Strb+/-)
	DDR Format	~680Mbps (Data0~n+/-, Clk+/-)
	Parallel Output:	~125MHz (CLKO, DO0~n<7:0>)
- 1.8V (Option: 2.8/3.3V) supply voltage (Option: 1.0 / 1.2 / 1.8V Logic/Level Shifter)
- Clock Edge Programmable (R\_F pin)
- MSB/LSB Programmable (SBS pin)
- ±150/200mV swing differential signal for low EMI
- Narrow bus reduces cable size
- Power Down Mode ~1μA (PD pin)

### Block Diagram

