

### Introduction

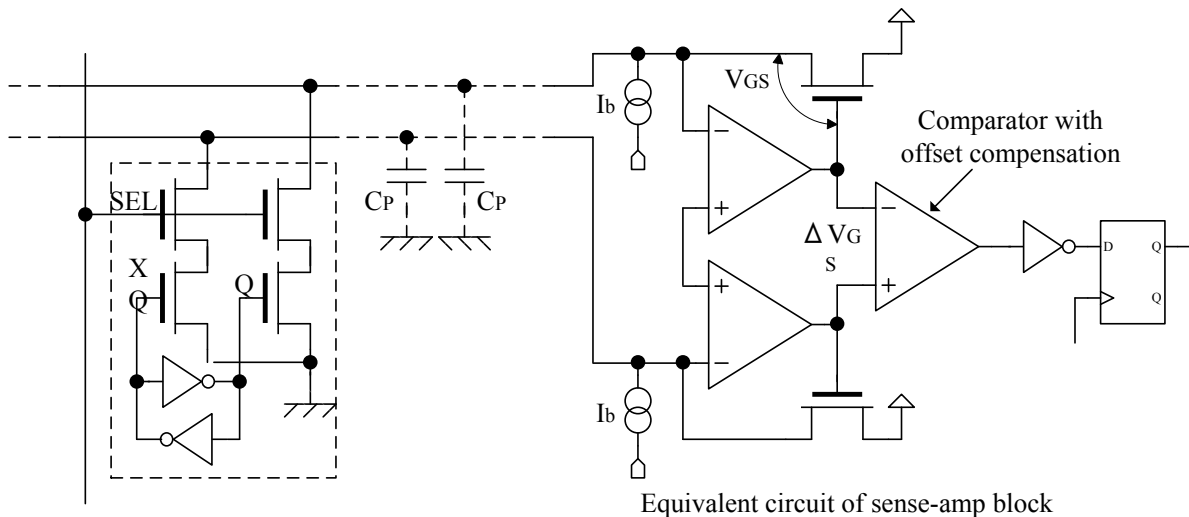
The PGA User Module implements an opamp based non-inverting amplifier with user-programmable gain. This amplifier has high input impedance, wide bandwidth, and selectable reference.

### Feature

- Power Voltage : 1.2V< (CMOS switch is possible for power range)
- Readout Rate : 250MHz< (Current consumption, Devices dependence)
- Current Consumption : 50uA (Readout-rate, Bit-line parasitic CAP ( $C_p$ ) dependence)
- Delay Time : 2nsec ( $C_p=2pF$ ), 3nsec ( $C_p=4pF$ ) (exclude effect of wire resistance)
- Control of timing is easy because pre-charge is unnecessary by the current detection type.
- Low power consumption is possible because it has only to be settling during 1 select.
- CMOS inverter composition is used as the first stage amplifier, and high-speed and low power consumption is realized.
- Offset cancel operation is done in blanking period, and faulty operation due to the element dispersion is prevented.
- This IP can use 90nm device low voltage of 1V.

### Equivalent Circuit

- The AB class amplification composition that low consumption power is possible is applied to each stage.
- A low power supply voltage operation is possible by circuit topology which can set up bit line potential optionally.



Equivalent circuit of sense-amp block  
Column A/D Data Readout Sense Amplifier Equivalent Circuit