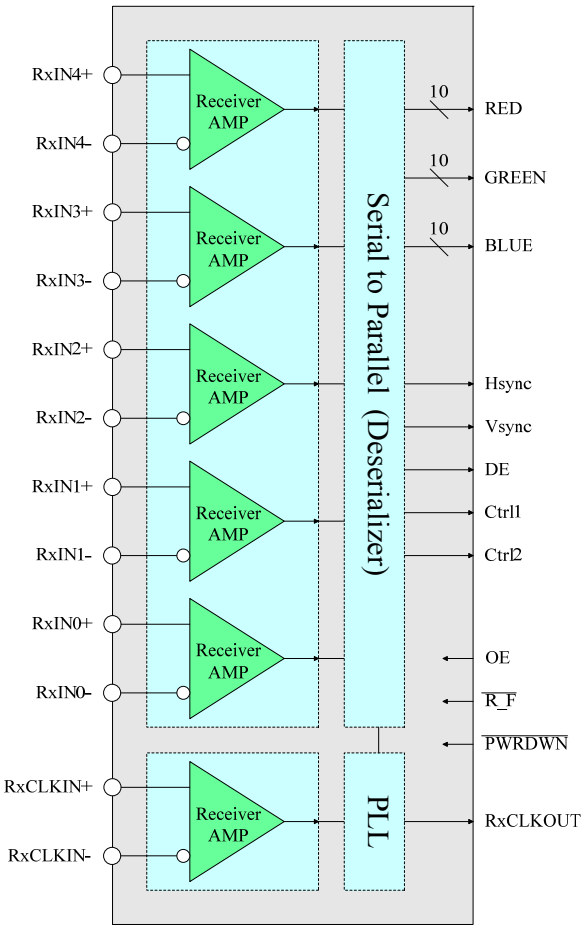
Introduction

The CL12482D receiver converts serial five LVDS data streams data back into parallel 35bits (30bits of RGB data and 5bits of HSYNC, VSYNC, DE and Control1, Control2) of LVCMOS parallel. The CL12482D receiver can be programmed for rising edge or falling edge clocks through a dedicated pin. The CL12482D receiver is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

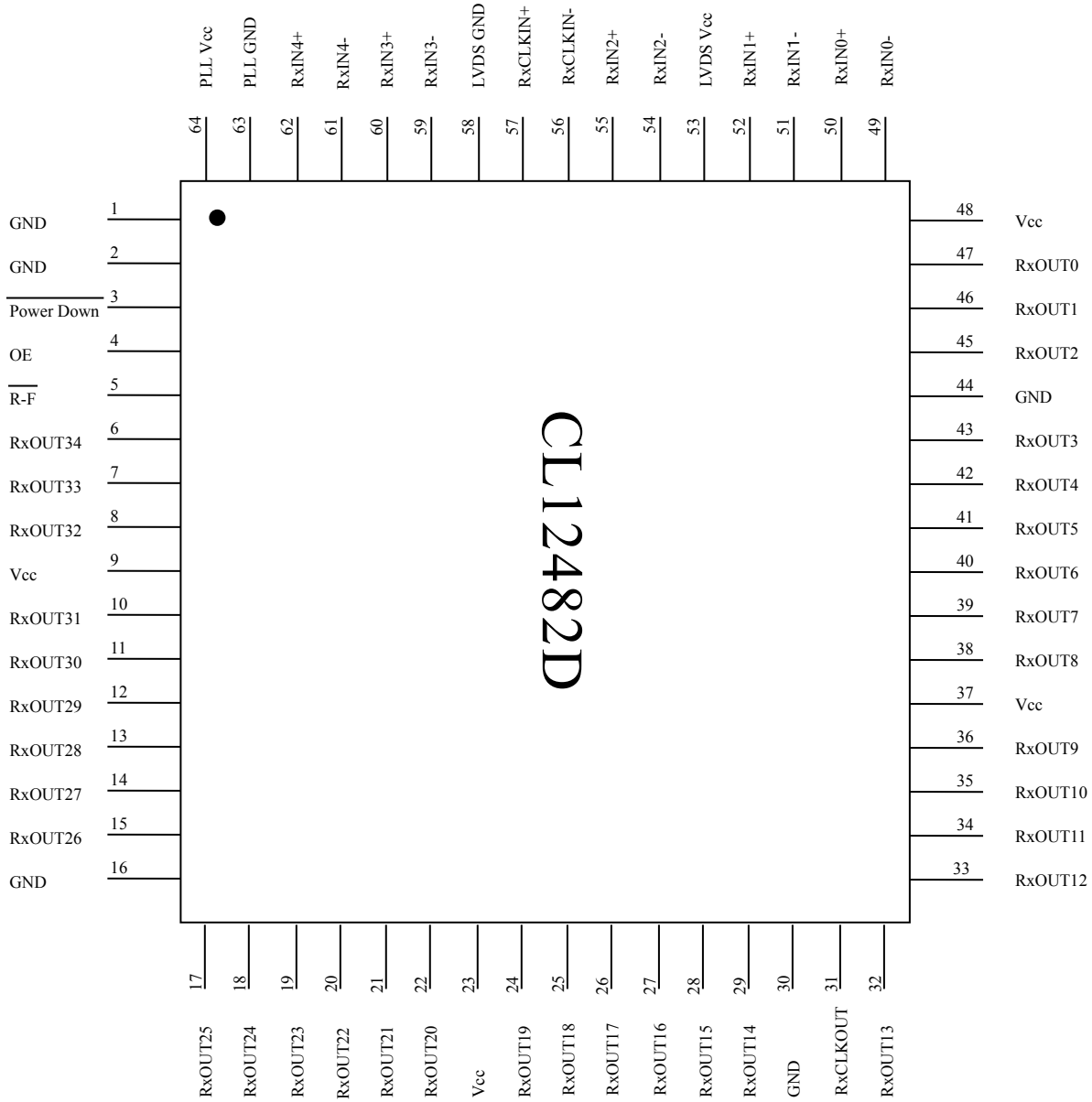
Feature

- Input Clock: 20MHz~85MHz Input Data Rate: 140Mbps~595Mbps
- Output Clock: 20MHz to 85MHz shift clock support
- Low power single 3.3V
- Clock edge programmable
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 64 Lead TQFP Package
- 345mV swing LVDS devices for low EMI
- Supports Fail-Safe function to all input channels
- Pin Compatible with THine THC63LVD104A

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description
RxOUT	35	OUT	LVCMOS Data Outputs
RxIN+	5	IN	Positive LVDS Differential Data Inputs
RxIN-	5	IN	Negative LVDS Differential Data Inputs
RxCLKOUT	1	OUT	LVCMOS Level Clock Output
RxCLKIN+	1	IN	Positive LVDS Differential Clock Input
RxCLKIN-	1	IN	Negative LVDS Differential Clock Input
$\overline{\text{Power Down}}$	1	IN	H: Normal Operation L: Power Down (All Outputs are Hi-Z)
$\overline{\text{R\_F}}$	1	IN	Programmable Strobe Select H: Rising Edge, L: Falling Edge
OE	1	IN	H: Normal Operation L: All outputs are Hi-Z
Vcc / GND	4/5	IN	Power Supply/Ground Pins for LVCMOS Inputs
PLL Vcc / PLL GND	1/1	IN	Power Supply/Ground Pins for PLL
LVDS Vcc / LVDS GND	1/1	IN	Power Supply/Ground Pins for LVDS Outputs

Control Signal Truth Table

$\overline{\text{Power Down}}$	$\overline{\text{R\_F}}$	OE	RxOUT	RxCLKOUT
0	0	0	All Outputs Hi-Z	Output Hi-Z
0	0	1	All ”0” Outputs	”0” Output
0	1	0	All Outputs Hi-Z	Output Hi-Z
0	1	1	All ”0” Outputs	”0” Output
1	0	0	All Outputs Hi-Z	Output Hi-Z
1	0	1	All Data Outputs	Falling Edge
1	1	0	All Outputs Hi-Z	Output Hi-Z
1	1	1	All Data Outputs	Rising Edge

Absolute Maximum Ratings

Supply Voltages	-0.3V to +4V
LVCMOS Input Voltage	-0.3V to (Vcc+0.3V)
LVCMOS Output Voltage	-0.3V to (Vcc+0.3V)
LVDS Receiver Input Voltage	-0.3V to (Vcc+0.3V)
Junction Temperature	+150 ℃
Storage Temperature	-65 ℃ to +150 ℃
Lead Temperature (Soldering, 4sec)	+260 ℃
Maximum Power Dissipation Capacity at 25℃	1.4 W

Electrical Characteristics

1. LVCMOS DC Specification — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions	min	typ	max	unit
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	
I_{IN}	Input Current	$V_{IN}=V_{CC}$,GND,2.5V or 0.4V		±5.1	±10	μA
V_{OH}	High Level Output Voltage	I_{OH}=-0.4mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}=12mA			0.8	

2. LVDS DC Specification — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions	min	typ	max	unit
V_{TH}	Differential Input High Threshold	V_{CM}=+1.2V			100	mV
V_{TL}	Differential Input Low Threshold		-100			
I_{IN}	Input Current	$0V \leqq V_{IN} \leqq V_{CC}$			±10	μA

3. Receiver Supply Current — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions		min	typ	max	unit
ICCRW	Receiver Supply Current	C_L=8pF Worst Case Pattern	f=65MHz		73	94	mA
			f=85MHz		83	96	
ICCRG		C_L=5pF 16Gray Scale Pattern	f=65MHz		40	54	
			f=85MHz		52	64	
ICCRZ		$\overline{\text{Power Down}}$=Low				10	μA

4. Switching Characteristics Vcc=3.0V to 3.6V Ta=-10°C to 70°C

Symbol	Parameter	min	typ	max	unit
RCOP	RxCLK OUT Period	7.41	T	50	ns
RCOH	RxCLK OUT High Time		T/2		
RCOL	RxCLK OUT Low Time		T/2		
CLHT	LVCMOS Low to High Transition Time		1	3	
CHLT	LVCMOS High to Low Transition Time		1	3	
$RSP_{OS}0$	Receiver Input Strobe Position for Bit 0	-0.5	0	+0.5	ns
$RSP_{OS}1$	Receiver Input Strobe Position for Bit 1	T/7-0.5	T/7	T/7+0.5	
$RSP_{OS}2$	Receiver Input Strobe Position for Bit 2	2T/7-0.5	2T/7	2T/7+0.5	
$RSP_{OS}3$	Receiver Input Strobe Position for Bit 3	3T/7-0.5	3T/7	3T/7+0.5	
$RSP_{OS}4$	Receiver Input Strobe Position for Bit 4	4T/7-0.5	4T/7	4T/7+0.5	
$RSP_{OS}5$	Receiver Input Strobe Position for Bit 5	5T/7-0.5	5T/7	5T/7+0.5	
$RSP_{OS}6$	Receiver Input Strobe Position for Bit 6	6T/7-0.5	6T/7	6T/7+0.5	
RSRC	RxOUT Setup to RxCLK OUT		T/2-2.5		ns
RHRC	RxOUT Hold to RxCLK OUT		T/2-2.5		
RCCD	RxCLK IN to RxCLK OUT Delay		4T/7		
RPLLS	Receiver Phase Lock Loop Set			10	ms
RPDD	Receiver Power Down Delay			1	us

Fail-Safe Function

The CL12482C/D receiver output ”high” when the differential inputs is :

1) Open
2) Undriven and Shorted
3) Undriven and Terminated

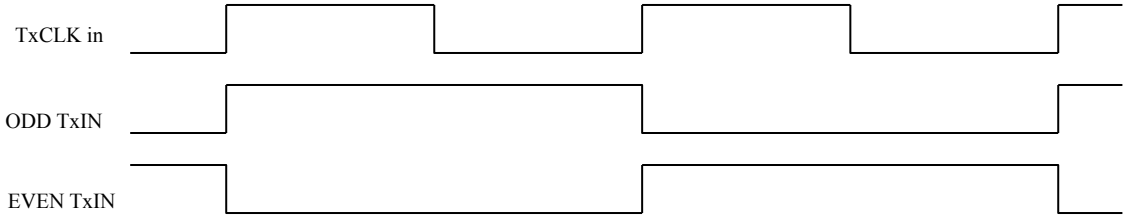


Fig.1 Worst Case Test Pattern

PIN Name	Signal	Signal Pattern	Signal Frequency
TxCLK IN	DOT CLK		f
TxIN28	R0		f/1024
TxIN29	R1		f/512
TxIN21	R2		f/256
TxIN22	R3		f/128
TxIN0	R4		f/64
TxIN1	R5		f/32
TxIN2	R6		f/16
TxIN3	R7		f/8
TxIN4	R8		f/4
TxIN5	R9		f/2
TxIN30	G0		f/1024
TxIN31	G1		f/512
TxIN23	G2		f/256
TxIN24	G3		f/128
TxIN6	G4		f/64
TxIN7	G5		f/32
TxIN8	G6		f/16
TxIN9	G7		f/8
TxIN10	G8		f/4
TxIN11	G9		f/2
TxIN32	B0		f/1024
TxIN33	B1		f/512
TxIN25	B2		f/256
TxIN26	B3		f/128
TxIN12	B4		f/64
TxIN13	B5		f/32
TxIN14	B6		f/16
TxIN15	B7		f/8
TxIN16	B8		f/4
TxIN17	B9		f/2
TxIN27	GND		Steady State, Low
TxIN18	HSYNC		Steady State, High
TxIN19	VSYNC		Steady State, High
TxIN20	DE		Steady State, High
TxIN34	GND		Steady State, Low

Fig.2 “1024-Grayscale” Test Pattern

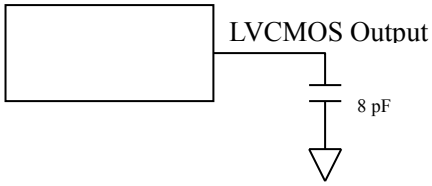


Fig.3: LVCMOS Output Load

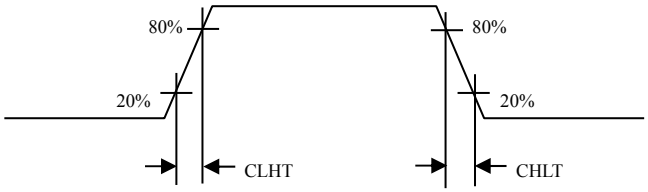


Fig.4: LVCMOS Output Transition Times

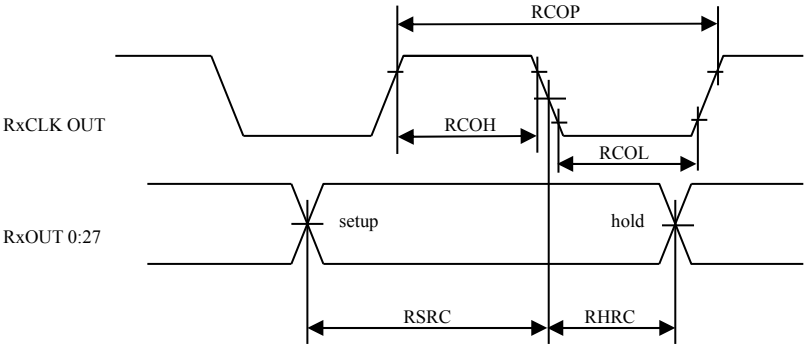


Fig.5: Receiver Setup/Hold and Low/High Times

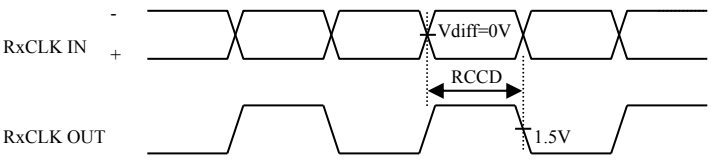


Fig.6: Receiver Clock in to Clock out Delay

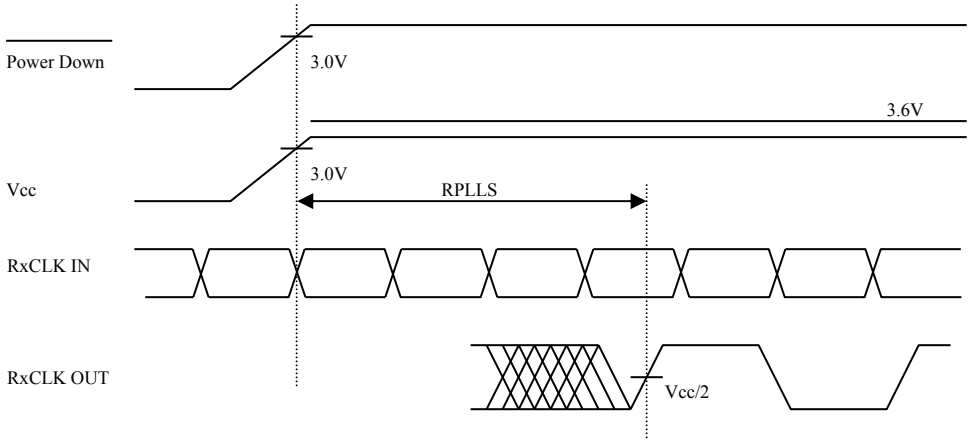


Fig.7: Receiver Phase Lock Loop Setup Time

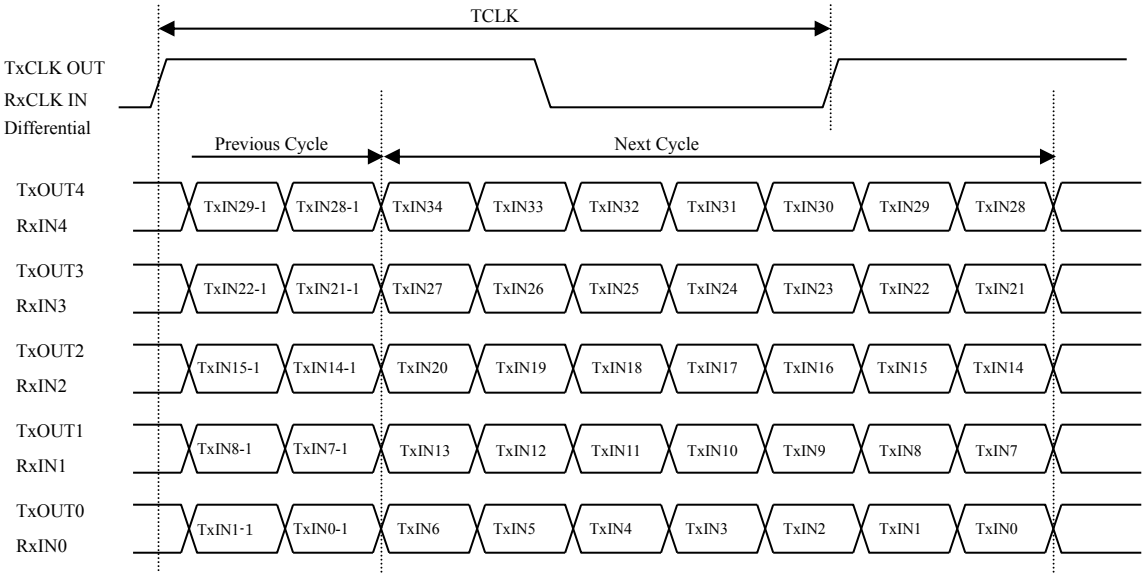


Fig.8: Parallel LVCMOS Data Inputs Mapped to LVDS Outputs

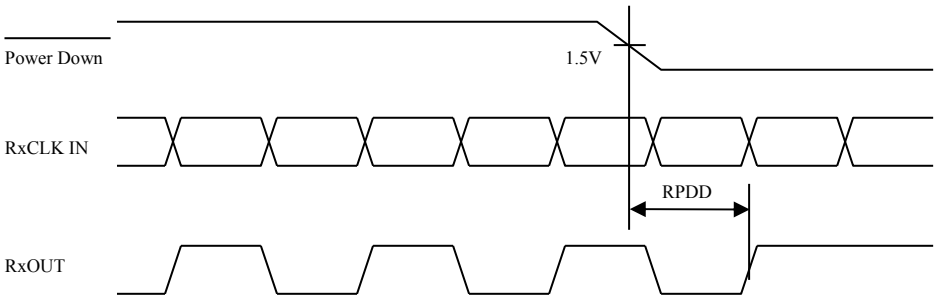


Fig.9: Receiver Power Down Delay

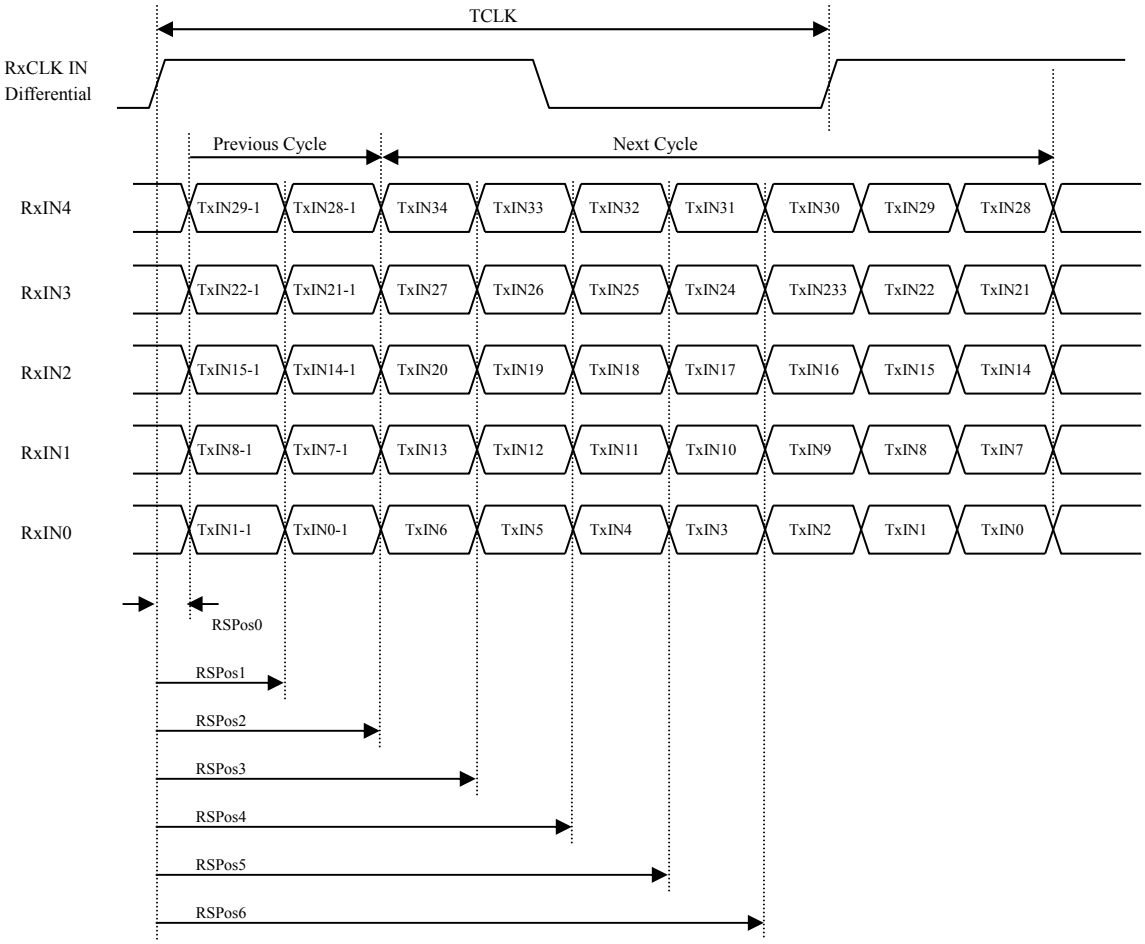


Fig.10: Receiver LVDS Input Strobe Position


CL12482D
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Modification History

Version	Date	Contents
1.00	2010 / 1 / 12	1) Block Diagram changed
0.40	2007 / 7 / 18	1) Input Clock frequency & Data rate added
0.30	2006 / 7 / 25	1) From CL12482C/D to CL12482D changed
0.20	2006 / 5 / 23	1) From CL12482A to CL12482C/D changed 2) Fail-Safe Function added 3) Package LOGO changed 4) Supply Current value changed 5) Maximum Dot Clock Frequency cjanged 6) I_{OL} value changed for Changing Frequency 7) The output Rising/Falling Time value changed 8) RxCLK OUT Cycle Time Changed
0.10	2005 / 5 / 10	Fig.2 Modified from 16-Gray to 1024-Gray
0.00	2004 / 4 / 27	First Version